What is claimed is:

1. A receiver for monitoring a serial ATA bus for the occurrence of an OOB signal, comprising:

a conventional Fiber Channel differential receiver having a parallel output;

a 10B decoder coupled to said parallel output and having an output at which a first signal appears which is set active by said 10B decoder when an illegal 10B pattern occurs in said shift register;

a pattern recognition circuit coupled to said parallel output and having an output at which a second signal appears which is set active by said pattern recognition circuit when a pattern of all logic 1s or all logic 0s appears in said register;

a state machine coupled to said first and second signals, for determining when said first and second signal have both been true for a predetermined amount of time and activating a third signal and for deactivating said third signal when either or both of said first and second signals go false;

a measurement timer for measuring the interval(s) during which said third signal is active; and

a pattern recognition circuit coupled to said measurement timer for analyzing the pattern of states of said third signal and the duration(s) of at least one of said states, and for drawing a conclusion as to whether an OOB signal has or has not occurred, and, if an OOB signal has occurred, for activating a fourth signal.

2. A process for detecting the transmission of an OOB signal on a serial ATA bus, comprising:

using a conventional Fiber Channel receiver to receive data on said bus;

analyzing said received data to determine if it contains an illegal 10B pattern, and, if so, activating a first signal;

analyzing said received data to determine if it contains a predetermined pattern of bits, and, if so, activating a second signal;

determining if said first and second signals are both active for more than a predetermined amount of time, and, if so, activating a third signal and keeping said third signal active as long as both said first and second signals are active; and

analyzing the duration(s) and pattern of the interval(s) when said third signal are active to determine if an OOB signal pattern is present.

3. A receiver apparatus to detect the presence of an predetermined signal pattern on a serial data bus, comprising:

a conventional differential or single ended receiver having its input(s) coupled to a bus upon which data or fill characters are normally constantly transmitted so as to maintain synchronization, said receiver having a parallel output at which received data appears;

a first decoder means for examining the data in said parallel output of said receiver and determining when said data represents an illegal pattern for normal data transmission of said bus and for outputting a first signal which is active when an illegal pattern has been detected;

a second decoder means for examining the data in said output register and determining when said data is a predetermined pattern such as all logic 1s or all logic 0s and for outputting a second signal which is active when said predetermined pattern is present;

means coupled to receive said first and second signals, for detecting when said first and second signals are both active for a time sufficiently long to be assured that the activation of both said signals is not an accident and may mean that said predetermined signal pattern is possibly starting, and for activating a third signal for a predetermined time; and

means coupled to said third signal for measuring the duration of predetermined states thereof and analyzing the pattern of said predetermined states and drawing a conclusion as to whether said predetermined signal pattern has occurred on said serial data bus or not, and, if so, for activating a fourth signal.

4. A process for determining if a reset signal comprised of a predetermined pattern of illegal common mode data transmissions have been transmitted on a serial format, differential signal data bus, comprising:

receiving data transmitted on said data bus using a conventional differential signal input receiver;

using high power pattern recognition circuitry which has been added to said conventional receiver at a point to be able to recognize illegal common mode input signals on said differential signal data bus and to time the duration of said common mode intervals;

using said high power pattern recognition circuitry to analyze the duration of each said common mode interval and the pattern of said common mode intervals and compare said pattern to a predetermine pattern of common mode intervals that defines said reset signal.

5. A receiver apparatus to receive high speed data transmitted on a bus and monitor for a bus reset signal comprised of any bit pattern or voltage condition on said bus which is illegal and never occurs during real data transmissions, comprising:

a high speed conventional receiver having one or more inputs coupled to said bus to receive high speed data transmitted on said bus, said receiver being capable of being powered down in sleep mode;

a low power pattern detection means coupled to said one or more inputs of said receiver for monitoring at all times for the occurrence on said bus of said bit pattern or voltage condition on said bus which is illegal and never occurs during real data transmissions, and upon detection thereof, for activating a signal which indicates a reset signal has been received.

6. A transmitter for transmitting an OOB signal on a differential serial ATA bus, comprising:

a conventional Fiber Channel transmitter having a parallel-in, serial-out input shift register coupled to its input and having first and

second differential outputs;

a first capacitor coupled to said first differential output for coupling said first differential output to a first transmit line on a differential serial ATA bus;

a second capacitor coupled to said second differential output for coupling said second differential output to a second transmit line on a differential serial ATA bus;

and wherein the values of said first and second capacitors are different from the coupling capacitors of a conventional Fiber Channel transmitter and have values selected in light of the termination resistance which terminates said differential serial ATA bus so as to establish an RC time constant which causes a decay on each transmit line from a differential signalling voltage level to a common mode voltage level within a predetermined time whenever an illegal data pattern of all logic 0s or all logic 1s is loaded into said input shift register.

7. A method for transmitting an OOB signal on a serial ATA differential signalling bus, comprising:

1) loading an illegal data pattern comprising all logic 1s or all logic 0s into an input shift register of a conventional fiber channel transmitter and continuing to load said illegal data pattern into said shift register for an interval equal to the duration of a first common mode interval of a OOB signal on a serial ATA bus;

2) loading any legal data pattern into said input shift register at the conclusion of step 1;

3) loading an illegal data pattern comprising all logic 1s or all logic 0s into an input shift register of a conventional fiber channel transmitter and continuing to load said illegal data pattern into said shift register for an interval equal to the duration of a second common mode interval of a OOB signal on a serial ATA bus;

4) loading any legal data pattern into said input shift register at the conclusion of step 3;

5) loading an illegal data pattern comprising all logic 1s or all

logic 0s into an input shift register of a conventional fiber channel transmitter and continuing to load said illegal data pattern into said shift register for an interval equal to the duration of a third common mode interval of a OOB signal on a serial ATA bus; and

6) loading any legal data pattern into said input shift register at the conclusion of step 5.